



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,487	12/30/1999	AZAR ASSADI	042390.P6880	6378

7590 06/30/2005  
Farzad E Amini  
Blakely Sokoloff Taylor & Zafman LLP  
12400 WILSHIRE BOULEVARD SEVENTH FLOOR  
LOS ANGELES, CA 90025

EXAMINER

HENN, TIMOTHY J

ART UNIT	PAPER NUMBER
----------	--------------

2612

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/475,487

Applicant(s)

ASSADI, AZAR

Examiner

Timothy J. Henn

Art Unit

2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 February 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8, 13-21 and 23-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8, 13-21 and 23-26 is/are rejected.
- 7) ☒ Claim(s) 7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 December 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-8, 13-21 and 23-26 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Objections***

2. Claims 1-4 are objected to because it is unclear how a protective layer can include a set of echelon diffraction gratings and at the same time be disposed between the adjacent echelon diffraction gratings of the set of echelon diffraction gratings.. Appropriate correction, such as deleting "the protective layer including" from lines 4 and 5 of claim 1, is required.

3. Claims 24 and 25 are objected to for being dependent on a cancelled claim. For the purposes of art rejection, claims 24 and 25 will be read as being dependent on claim 17. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-6, 8 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thiel et al. (US 6,114,739) in view of Gal et al. (US 5,600,486) in view of Kato et al. (US 2002/0030890).

**[claim 1]**

Regarding claim 1, Thiel discloses a set of light sensitive diodes including a transparent conductor (Figure 2, Item 50), the set of light sensitive diodes including an n-layer (Figure 2, Item 44); an i-layer (Figure 2, Item 46) and a p-layer (Figure 2, Item 48). However, Thiel does not disclose a set of echelon diffraction grating elements for producing complementary colors.

Gal discloses the use of echelon diffraction grating elements placed above an image sensor (Figure 2). Gal discloses the use of these diffraction gratings to separate light into color spots for a camera on a chip (c. 2, ll. 1-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the protective layer of Gal in the camera of Thiel to separate light into its respective colors for creation of color images. However, Thiel in view of Gal does not disclose a protective layer placed above the transparent conductor and disposed between adjacent echelon diffraction gratings.

Kato discloses that by placing antireflection coatings on a diffractive optical element the diffraction efficiency of the optical element can be improved (Figure 11; Paragraphs 0082-0083). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an antireflection coating above the echelon diffraction grating elements of Thiel in view of Gal to improve the devices diffraction efficiency. The examiner notes that by placing an antireflection coating on the echelon diffraction gratings of Thiel in view of Gal, they would necessarily be above the transparent conductor 50 and between adjacent echelon grating elements as

Art Unit: 2612

claimed.

**[claim 2]**

Regarding claim 2, see claim 1.

**[claim 3]**

Regarding claim 3, Thiel discloses an image sensor that is compatible with a metal oxide semiconductor (MOS) fabrication process and which generates charges representative of the intensity of incident light (c. 3, ll. 27-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use materials which are compatible with MOS fabrication processes for construction of the echelon diffraction gratings of Gal and the antireflection coating of Kato.

**[claim 4]**

Regarding claim 4, Gal discloses the use of four step echelon grating elements in Figures 14-18.

**[claim 5]**

Regarding claim 1, Thiel discloses an integrated pixel sensor structure having: a set of light sensitive diodes including a transparent conductor (Figure 2, Item 50), the set of light sensitive diodes including an n-layer (Figure 2, Item 44); an i-layer (Figure 2, Item 46) and a p-layer (Figure 2, Item 48) and a post capture signal processing circuit coupled to the integrated pixel sensor (c. 3, ll. 2-10). However, Thiel does not disclose a set of echelon diffraction grating elements for producing complementary colors.

Gal discloses the use of echelon diffraction grating elements placed above an image sensor (Figure 2). Gal discloses the use of these diffraction gratings to separate

Art Unit: 2612

light into color spots for a camera on a chip (c. 2, ll. 1-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the protective layer of Gal in the camera of Thiel to separate light into its respective colors for creation of color images. However, Thiel in view of Gal does not disclose a protective layer placed above the transparent conductor and disposed between adjacent echelon diffraction gratings.

Kato discloses that by placing antireflection coatings on a diffractive optical element the diffraction efficiency of the optical element can be improved (Figure 11; Paragraphs 0082-0083). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an antireflection coating above the echelon diffraction grating elements of Thiel in view of Gal to improve the devices diffraction efficiency. The examiner notes that by placing an antireflection coating on the echelon diffraction gratings of Thiel in view of Gal, they would necessarily be above the transparent conductor 50 and between adjacent echelon grating elements as claimed.

**[claim 6]**

Regarding claim 6, see claim 5.

**[claim 8]**

Regarding claim 8, Gal discloses the use of four step echelon grating elements in Figures 14-18.

**[claims 13-16]**

Claims 13-16 are method claims corresponding to apparatus claims 1-4.

Therefore, claims 13-16 are analyzed and rejected as previously discussed with respect to claims 1-4.

6. Claims 17-21, 23, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thiel et al. (US 6,114,739) in view of Rostoker (US 5,760,834).

**[claim 17]**

Regarding claim 17, Thiel discloses an integrated circuit die (Figure 2) comprising: an image sensing area of the die having a plurality of light-sensitive diodes (Figure 2, Items 44, 46 and 48) formed above a metallization layer of the die (Figure 2, Items 45) and having a transparent conductor (Figure 2, Item 50). However Thiel lacks a protective layer of the die and includes a plurality of echelon diffraction gratings and wherein the protective layer has a low enough deposition temperature so as not to environmentally stress the transparent conductor, and the protective layer covers a portion of the transparent layer not covered by the plurality of echelon diffraction gratings.

Rostoker teaches that by placing elements including a LCD panel (Figure 16B, Item 1630) and a binary optic element or "diffraction grating element" (Figure 16B, Item 1610) over an image sensing array (Figure 16B, Item 1620) a sandwiched display/image sensor (c. 13, ll. 40-65; c. 14, ll. 23-39) capable of color imaging (c. 10, ll. 9-43) is formed. The examiner notes that Rostoker's LCD panel placed above an image sensing array inherently form a protective layer which covers the entire array and the

Art Unit: 2612

set of echelon diffraction grating elements, including an area which would not be covered by the echelon diffraction grating elements as claimed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a "protective layer" or LCD panel and a binary optic element as taught by Rostoker to create a combination display/image sensor capable of color imaging. The examiner further notes that in order for such a device to be manufactured the protective layer must inherently have a low enough deposition temperature so as not to environmentally stress the transparent conductor.

**[claim 18]**

Regarding claim 18, Thiel discloses a plurality of diodes having amorphous silicon as their photoactive material (Figure 2, Item 46).

**[claim 19]**

Regarding claim 19, Thiel discloses a plurality of diodes having a n-i-p structure (Figure 2, Items 44, 46 and 48).

**[claim 20]**

Regarding claim 20, Thiel discloses n and p layers which are thin relative to the i portion (Figure 2).

**[claim 21]**

Regarding claim 21, Thiel discloses a plurality of diodes having a transparent conductor made of an ITO layer that forms a top contact of the plurality of diodes (Figure 2, Item 50; c. 5, ll. 38-45).

**[claim 23]**



Regarding claim 23, Theil in view of Rostoker lacks a protective layer including anti-reflection properties. Official Notice is taken that the use of anti-reflection layers in image sensors is notoriously well known to improve the efficiency of the image sensors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include anti-reflection properties in the protective layer of Theil in view of Rostoker to improve the efficiency of the image sensor.

**[claim 24]**

Regarding claim 24, Rostoker discloses a diffraction grating designed to impart RGB color sensing to the image sensing area of the die (Figure 8; c. 10, ll. 9-43).

**[claim 25]**

Regarding claim 7, Rostoker discloses the use of spin-on glass or "sol-gel" for forming the diffractive optical elements which are included in the protective layer as claimed (c. 5, l. 47 - c. 6, l. 12; c. 9, ll. 58-66; c. 13, ll. 20-65).

**[claim 26]**

Regarding claim 26, Rostoker discloses the use of imaging devices such as CCD arrays or "any other suitable device which changes state or generates a potential or potential difference upon incidence of light" (c. 5, ll. 5-26). Thiel discloses an image sensor that is compatible with a metal oxide semiconductor (MOS) fabrication process and which generates charges representative of the intensity of incident light (c. 3, ll. 27-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use materials which are compatible with MOS fabrication processes for construction of the protective layer of Rostoker when using "any other

suitable device which changes state or generates a potential or potential difference upon incidence of light” such as MOS image sensors.

***Allowable Subject Matter***

7. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**[claim 7]**

Regarding claim 7, the prior art does not teach or fairly suggest a protective layer as claimed which is made of a sol-gel material.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

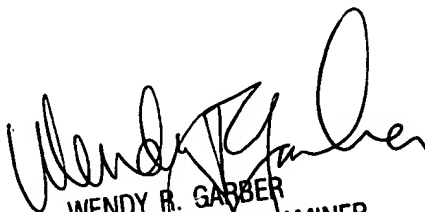
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Henn whose telephone number is (571) 272-7310. The examiner can normally be reached on M-F 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJH  
6/20/2005

  
WENDY R. GARBER  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600